METHOD AND SYSTEM FOR RE-TARGETING INTEGRATED CIRCUITS

ABSTRACT

The present invention allows a designer to easily re-target the design optimized for the device of one integrated circuit vendor to the device of another vendor. The designer can start with a set of post-routed boolean equations optimized for a certain target integrated circuit. The present invention allows the automatic generation of a synthesizable, editable, and simulatable HDL description. The designer may edit the HDL code. Another target may be selected. Design optimization and placement and routing can be performed for the new target.